

FIG. 1

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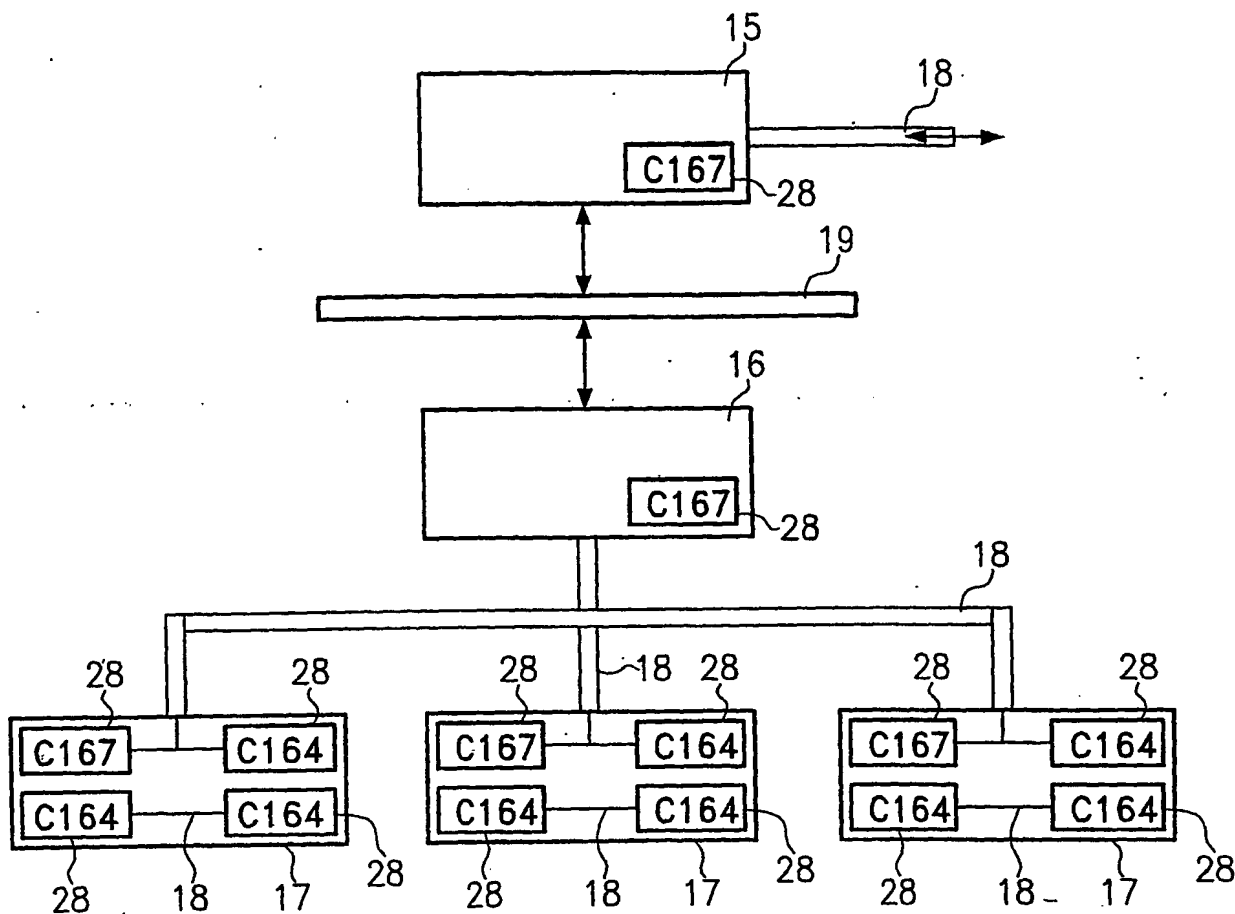


FIG. 2

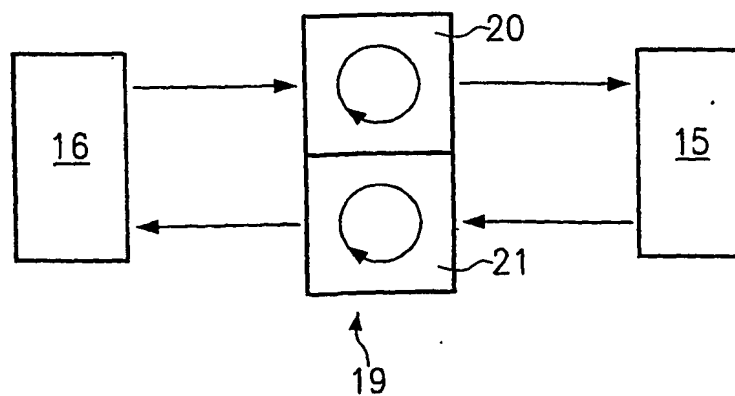


FIG. 3

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FIG.4

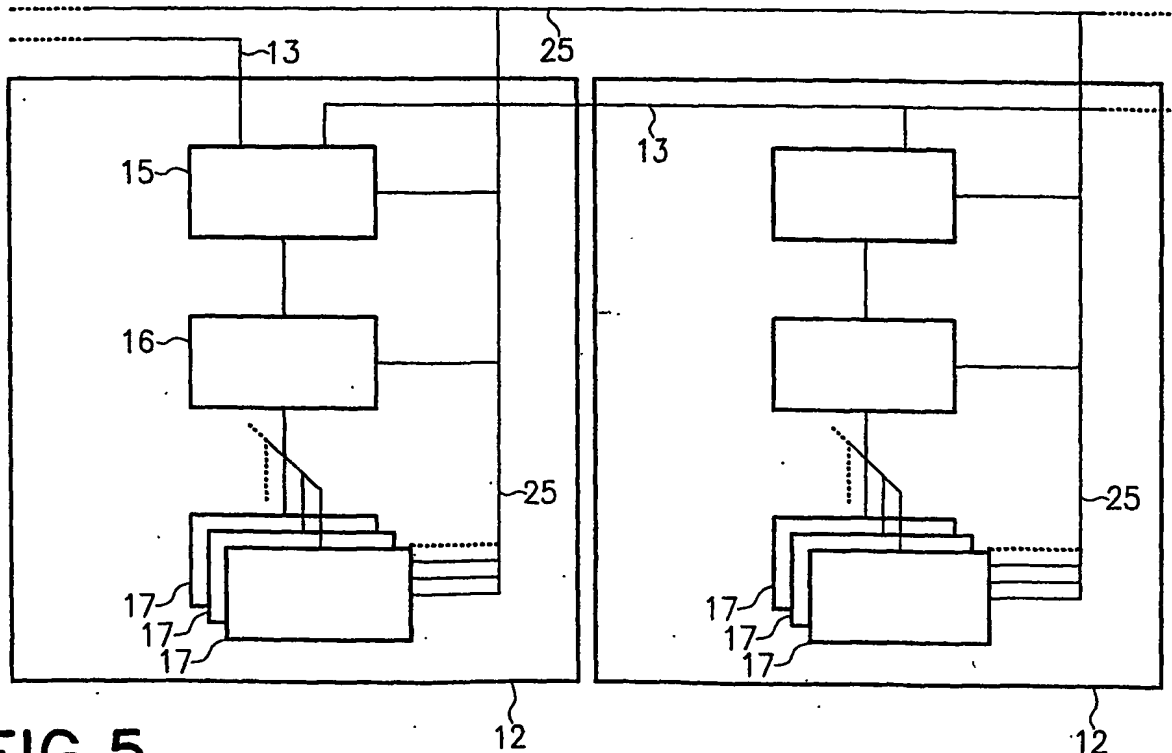
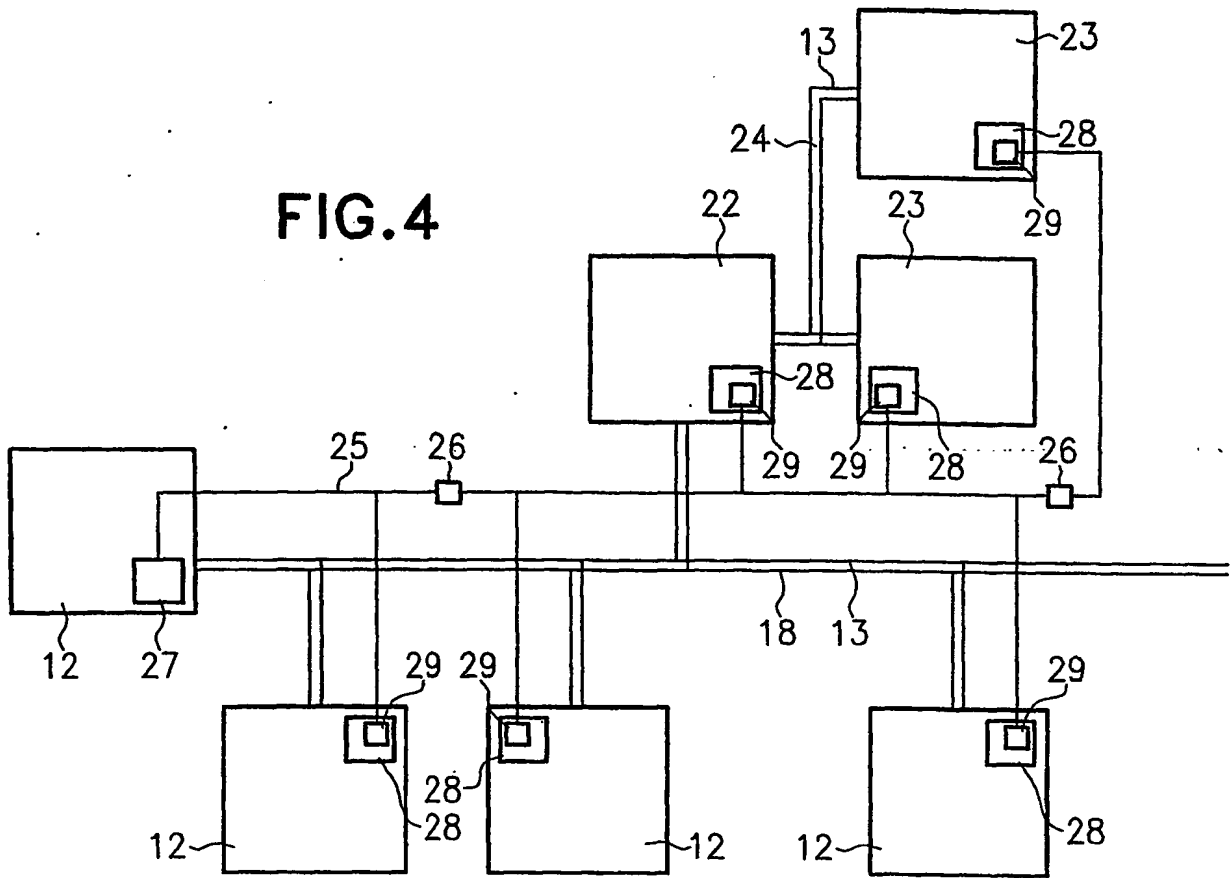


FIG.5

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PI VW	1	PI SM PCB3 SAT3	20	PI2 SM PCB2 SAT2	39
PI RT	2	PI1 SM PCB1 BM	21	PI2 SM PCB2 SAT3	40
PI1 VW	3	PI1 SM PCB1 SAT1	22	PI2 SM PCB3 BM	41
PI1 RT	4	PI1 SM PCB1 SAT2	23	PI2 SM PCB3 SAT1	42
PI2 VW	5	PI1 SM PCB1 SAT3	24	PI2 SM PCB3 SAT2	43
PI2 RT	6	PI1 SM PCB2 BM	25	PI2 SM PCB3 SAT3	44
PI3 VW	7	PI1 SM PCB2 SAT1	26	PI3 SM PCB1 BM	45
PI3 RT	8	PI1 SM PCB2 SAT2	27	PI3 SM PCB1 SAT1	46
PI SM PCB1 BM	9	PI1 SM PCB2 SAT3	28	PI3 SM PCB1 SAT2	47
PI SM PCB1 SAT1	10	PI1 SM PCB3 BM	29	PI3 SM PCB1 SAT3	48
PI SM PCB1 SAT2	11	PI1 SM PCB3 SAT1	30	PI3 SM PCB2 BM	49
PI SM PCB1 SAT3	12	PI1 SM PCB3 SAT2	31	PI3 SM PCB2 SAT1	50
PI SM PCB2 BM	13	PI1 SM PCB3 SAT3	32	PI3 SM PCB2 SAT2	51
PI SM PCB2 SAT1	14	PI2 SM PCB1 BM	33	PI3 SM PCB2 SAT3	52
PI SM PCB2 SAT2	15	PI2 SM PCB1 SAT1	34	PI3 SM PCB3 BM	53
PI SM PCB2 SAT3	16	PI2 SM PCB1 SAT2	35	PI3 SM PCB3 SAT1	54
PI SM PCB3 BM	17	PI2 SM PCB1 SAT3	36	PI3 SM PCB3 SAT2	55
PI SM PCB3 SAT1	18	PI2 SM PCB2 BM	37	PI3 SM PCB3 SAT3	56
PI SM PCB3 SAT2	19	PI2 SM PCB2 SAT1	38		

FIG.6

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endg. Empfänger Sender	cs_noexist_proc	PI_VW	PI_RT	PI1_VW	PI1_RT
/*cs_noexist_proc*/	{{ 0 , 0 }},	{ 0 , 0 },	{ 0 , 0 },	{ 0 , 0 },	{ 0 , 0 },
/* PI_VW */	{{ 0 , 0 }},	{B_MSG, 0 },	{B_DPR, PI_RT},	{B_CAN, PI1_VW },	{B_CAN, PI1_VW }, ...
/* PI_RT */	{{ 0 , 0 }},	{B_DPR, PI_VW},	{B_MSG, 0 },	{B_DPR, PI_VW },	{B_DPR, PI_VW}, ...
/* PI1_VW */	{{ 0 , 0 }},	{B_CAN, PI_VW },	{B_CAN, PI_VW },	{B_MSG, 0 },	{B_DPR, PI1_RT }, ...
/* PI1_RT */	{{ 0 , 0 }},	{B_DPR, PI1_VW },	{B_DPR, PI1_VW },	{B_DPR, PI1_VW },	{B_MSG, 0 }, ...
/* PI2_VW */	{{ 0 , 0 }},	{B_CAN, PI_VW },	{B_CAN, PI_VW },	{B_CAN, PI1_VW },	{B_CAN, PI1_VW }, ...
/* PI2_RT */	{{ 0 , 0 }},	{B_DPR, PI2_VW },	{B_DPR, PI2_VW },	{B_DPR, PI2_VW },	{B_DPR, PI2_VW }, ...
/* PI3_VW */	{{ 0 , 0 }},	{B_CAN, PI_VW },	{B_CAN, PI_VW },	{B_CAN, PI1_VW },	{B_CAN, PI1_VW }, ...
/* PI3_RT */	{{ 0 , 0 }},	{B_DPR, PI3_VW },	{B_DPR, PI3_VW },	{B_DPR, PI3_VW },	{B_DPR, PI3_VW }, ...
/* PL_SM_PCB1_BM */	{{ 0 , 0 }},	{B_CAN, PI_RT },	{B_CAN, PI_RT },	{B_CAN, PI_RT },	{B_CAN, PI_RT }, ...
/* PL_SM_PCB1_SAT1 */	{{ 0 , 0 }},	{B_CAN, PI_RT },	{B_CAN, PI_RT },	{B_CAN, PI_RT },	{B_CAN, PI_RT }, ...

FIG.7